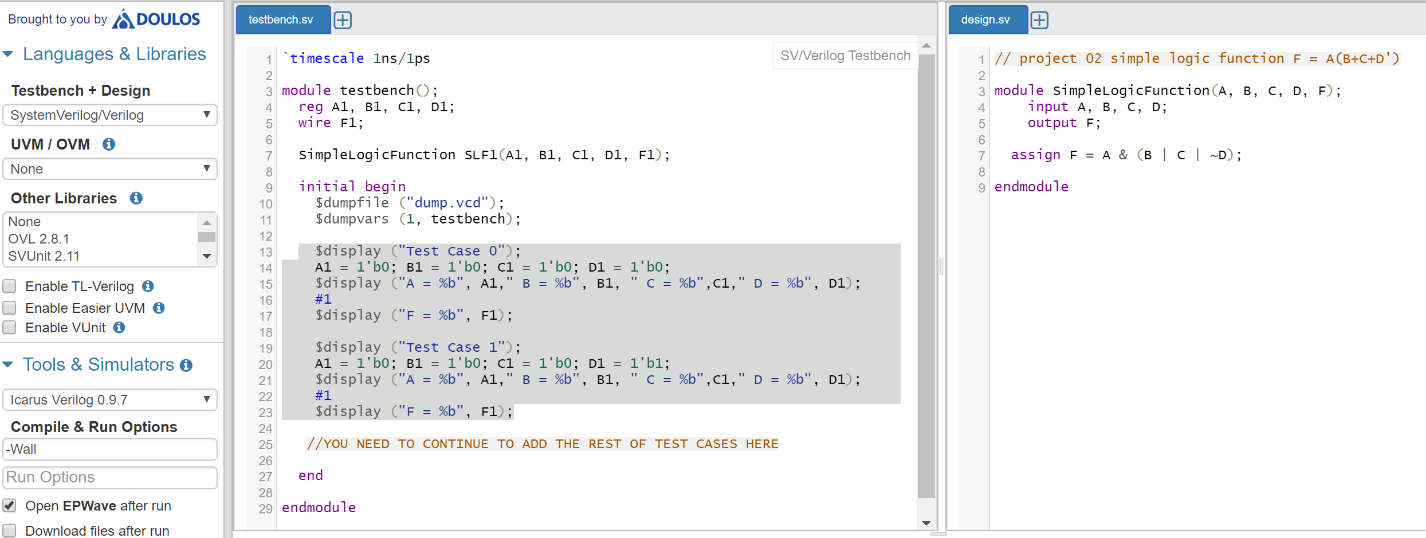
LAB 02: **Simple Logic Function *F = A(B+C+D’)***

# Objectives:

* **Continue to get familiar with EDAPlayground**
* **Similar to the tutorial/lab01, this project asks you to repeat the same procedures to create Verilog module, to write testbench code, and to generate the simulation waveform for the above given logic function.**
* **Things** needed to turn in (combine everything into a single word file)
  + Truth table/Function Talbe for function F showing all combinations (continue to derive values of F for the remaining combinations)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F**  **F** |
| 0 | 0 | 0 | 0 | **0**  **0** |
| 0 | 0 | 0 | 1 | **0**  **0** |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

* + Verilog module code in EDAPlayground (screenshot or copy of the verilog code)



* + Verilog testbench code (screenshot or copy of the verilog code)

$display ("Test Case 0");

A1 = 1'b0; B1 = 1'b0; C1 = 1'b0; D1 = 1'b0;

$display ("A = %b", A1," B = %b", B1, " C = %b",C1," D = %b", D1);

#1

$display ("F = %b", F1);

$display ("Test Case 1");

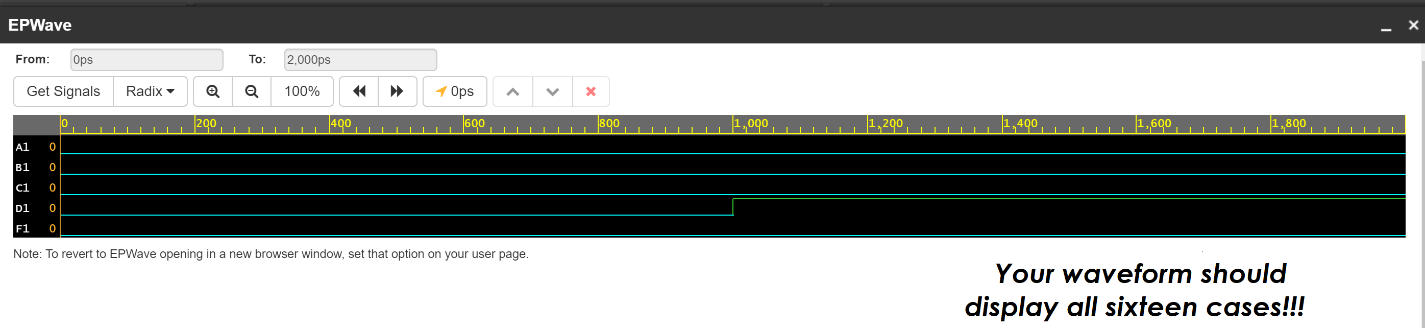
A1 = 1'b0; B1 = 1'b0; C1 = 1'b0; D1 = 1'b1;

$display ("A = %b", A1," B = %b", B1, " C = %b",C1," D = %b", D1);

#1

$display ("F = %b", F1);

* + Simulation waveforms (I only show TWO cases here. Your waveforms should show all SIXTEEN cases!!!)



**Finally**, upload report to the project Dropbox in beachboard (refer to EDAPlayground Tutorial for report guidance)!